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Physics

Basic Advantages of Integrated Circuits Made on the Structure of "Silicon on Sapphire"(SOS)

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ABSTRACT. Development of an integrated circuit using silicon on sapphire (SOS) structures, namely, constant memory device, fulfilled on the basis of vertical diode structure, is described. An optimal technological route of creation of a diode matrix on SOS with account of obtaining isolated "islets" of silicon parameters of matrix is introduced. Complete technological cycle of diode integrated circuits on SOS is given. The obtained diode matrix was used in constant memory blocks of radioelectron devices for space and submarine apparatus.

Interesting assumptions about the prospective of exploitation of SOS structures in nanoelectronics in order to create solid state optoelectronic devices using nanosilicon in SOS structures are reported. *© 2010 Bull. Georg. Natl. Acad. Sci.*

Key words: *sapphire substrate, diode matrix, nanosilicon.*

The experience of elaboration of planar technology on silicon monocrystals with the aim of creation of circuits of different structures and functional application shows that practically the basic part of silicon monocrystal fulfills the role of mechanical substrate. It is shown that if the integrated circuits are made in a thin layer of epitaxial silicon film, grown on monolithic silicon crystal, their parameters are significantly better, as the epitaxial layer is characterized by much less quantity of defects compared with a monolithic layer. In this case monolithic silicon presents a neutral (passive) substrate, and epitaxial silicon layer is an active part of the structure.

In this connection in microelectronics the structure of silicon on dielectrics (SOD), in which the substrate of monolithic silicon is changed by different dielectrics, has been developed. Among the above-mentioned structures heterostructures of "silicon on sapphire" (SOS) are especially prospective. Such structures represent a thin epitaxial layer of silicon, grown on the respectively chosen oriented plane of sapphire (Al_2O_3), which serves as a substrate for the integrated circuit [1] made in epitaxial silicon layer (Fig. 1).

Complete isolation of active and passive components, exclusion of substrate influence and absence of current leakage easily occur in such structure. Vertical p-n transitions provide minimization of parasite capacity, stability to radiation, temperature, chemical and other possible effects. The circuits are characterized by small power consumption, high action rate and reliability.

In order to determine the advantages of heterostructure (SOS) exploitation, an electrically programmed constant memory device, made on the basis of vertical diode structures, was chosen by us as the object of investigation [2]. The circuit contains mutually perpendicular transmission bands (crossing commutation). In the places of mutually perpendicular bands crossing the diode structure with "jumper" is formed. During the transmission of electric impulse of a definite quantity "the jumper" melts, as a result of which the

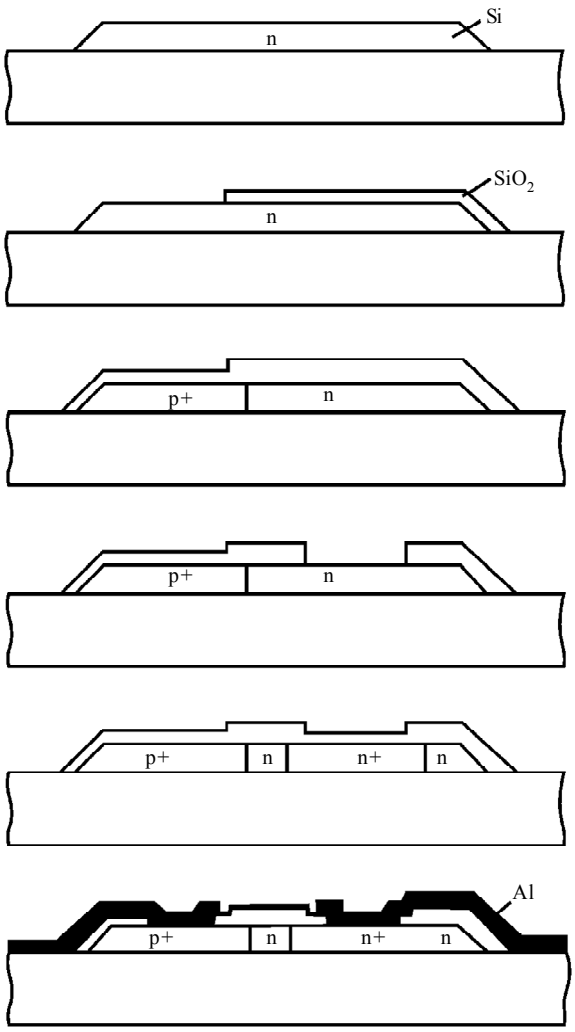

Fig. 1. Series of the main technological operations at creation of SOS–diodes with facing p-n transition

chosen diode is switched off from the matrix, providing the appearance of logical zero at a certain place of the matrix. The design of matrix has been chosen with account of both schematic requirements and technological potentialities. Therefore the primary task was to choose and work out individual technological processes taking into account their peculiarities of occurrence in SOS structures in order to select an optimal technological route of diode matrix on SOS creation on the basis of typical equipment used in planar technology on monolithic silicon.

The main advantage of diode (or diode component of integrated circuit) on SOS structure is small electrical capacity. It is composed of the capacity of p-n transition and mutual capacity of anode and cathode current conductive sections. To decrease both components of capacity small "islets" of silicon are formed on sapphire and by means of diffusion of acceptor and donor impurities through the whole thickness of the silicon film the facing p-n transition is formed (Fig. 1).

For electrical isolation of different matrix layers we used the oxide of SiO_2 grown on heteroepitaxial layer of SOS structure as the result of interaction in conditions of high temperature between oxygen and epitaxial silicon layer.

Sapphire substrate is more stable to chemical, radiation and temperature impacts compared with the silicon layer (the melting temperature of silicon is 1412ºC, while for sapphire it is 2040ºC).

The technology of growing SiO_2 layer for application as the isolating layer is practically identical to the corresponding processes for the usual planar technology on monolithic silicon. To create emitter (p^+ layer) and collector layers (n^+ layers) doping with the corresponding diffusants was used (Fig. 2). The value of the surface resistance was chosen in order to obtain low ohm contact metal/semiconductor. Optimal regimes for obtaining oxide isolation layers were also determined. Some detailed technological parameters of manufacture of diode matrix are listed below:

- the first oxidation is conducted before boron diffusion in order to get oxide thickness 0.4±0.05 mkm;
- the second oxidation is conducted before phosphorus diffusion in order to get oxide thickness 0.5±0.05 mkm;
- the third oxidation is conducted for isolation of conductive bands in order to get oxide thickness 0.7±0.05 mkm.

To create emitter (p^+ region, Fig. 2) and collector regions (n^+ region), and current conductive lines diffusion process was used. Boron diffusion into emitter regions was carried out at the temperature 1080ºC. Liquid boron bromide (BBr_3) was used as diffusant, the process was conducted for 30 minutes. This regime provided contact resistance R=15-20 ohm/□.

To create collector regions and silicon current conductive lines phosphorus diffusion was used. The regime was as follows: temperature 1100ºC, time – 50 min. Such regime provided contact resistance R=1.2-1.3 ohm/□. Phosphorus chloride PCl_3 was used as diffusant.

Creation of isolated silicon "islets" is one of the main points in SOS technologies. The main requirements are: presentation of the exact geometrical sizes defined by the construction, and specific for SOS technology, providing the necessary size of flatness of silicon islets. With this aim, different silicon solvents were used, such as KOH with anisotropic property, possessing a low rate of silver glycol etching, solution of nitrogen (HNO_3) and hydrogen fluorine (HF) acids.

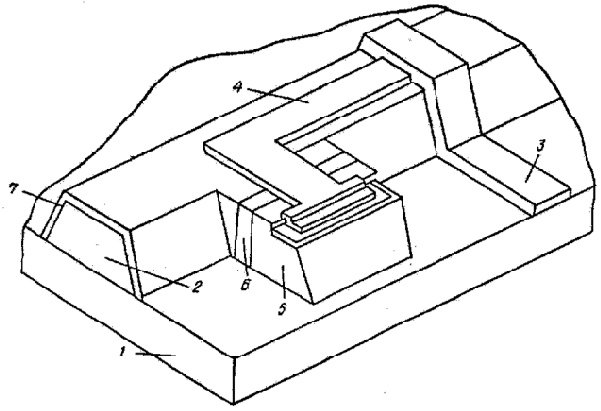

Fig. 2. Fragment of diode matrix. 1 - substrate; 2, 3 – conductive rubbers: doped with phosphorus silicon (2) and aluminum (3) lines perpendicular to it; 4 – Jumper made of thin aluminum, passing through p-n transition; 5 – p-type area; 6 – n-type region; 7 – oxide isolation layer.

The most acceptable results were obtained while conducting the process of photolithography directly on silicon islet without application of interlayers. In this case flatness of the islets' boundaries is naturally obtained, as the boundary between the silicon-photoresist is subjected to the influence of solvents longer than the lower layers at the boundary with sapphire. The objective index of flatness of slopes was the interferential lines continuity control in the region of grades silicon – sapphire.

The complete technological cycle of creation of diode integral scheme on SOS involves six photolithography processes: three on the SiO_2 layer, one – on the silicon layer, and two – on the aluminum. Each photolithography was produced by the standard for silicon planar technology tour:

1. Application of photoresist (ФП-383 sensitivity 400 lines/mm) by the method of centrifuging. Photoresist layer thickness ≈1 mkm;
2. Drying in thermostat. Regime: temperature - 90ºC, time – 20 minutes;
3. Alignment and exposure by ultra-violet rays;
4. Development in 3% water solution KOH;
5. Temperature treatment at 140ºC for 40 minutes to improve bonding between photoresist and the surface;
6. Opening of the regions defined by the topology to the corresponding solvents;
7. Removal of the residues of photoresist and chemical treatment.

It is necessary to note, as our experience showed, that the photolithographic processes on the SOS with individual islets practically do not differ from the processes conducted on monolithic silicon in the case when the boundaries of the islets are sloping.

The problem of diode matrix programming, or more precisely, the introduction of a definite double coding system information into the matrix is a very important point. In our case, logical "1" corresponds to the presence of diode with undestroyed jumper in the place of crossing of bus (doped with phosphorus bus duct and perpendicular to it aluminum line), and logical "0" – with melted jumper. For a jumper we used a thin strip of Al, going through the p-n transition. This fact allowed us practically to reduce false information recording down to zero.

Below we introduce some constructive data of diode matrix, elaborated by us: Capacity of facing vertical transition equals 0.01-0.02 pF, area of transition 1-2 mkm^2. The total capacity of the diode component does not exceed 0.05 pF, direct current 15 milliampere, input voltage of information is ≤ 20V. Diode matrix 712 PB1 contains 16 lines and 20 columns (4 reserved columns), information capacity is 256 bits.

On the basis of the above short description of the technological processes of diode matrix on SOS for a number of years at the plant of Scientific Research Institute "MION" the production of electrically programmed diode matrix (712 PB1 and others) has been implemented. They were used in the blocks of constant memory radioelectronic devices in space apparatuses, also in submarines. Our paper is the first in the free access publication, in which we describe the details of construction and technology of devices on SOS, diode matrix in particular.

The advantages of integrated circuits on SOS structures, described in the paper, found their local functional direction of SOS IS in microelectronics.

One more interesting field of application of SOS structures is optoelectronics. This means that the creation of both radiating light elements and photodetector is possible on sapphire substrate. Due to transparency of sapphire in a wide range of radiation spectrum, it will allow us to create variants of solid state original optopairs [3,4].

Recently the abilities of nanostructurized silicon to light emission attracted the attention of many investigators. The researches in this direction are developed mainly in the field of components for nanooptoelectronics. Basing on the published works [5], also WEB publications, prospective application of nanosilicon and processes on its basis are predicted such as: silicon emitters for integral optical schemes, in memory devices, as light-wave components, matrix emitters and optopairs, lasers, etc. It is quite tempting to use nanosilicon while making optoelectronic devices on the basis of SOS struc-

tures, as creation of sapphire nanosilicon emitters and photodetectors will give us the possibility to work out prospective solid state optoelectronic devices (as well as matrix type) for different fields of technology.

Proceeding from the above, development of work on the use of SOS structures in nanosilicon is a very important task in sophisticated micro- and optoelectronics.

ფიზიკა

"სილიციუმი საფირონზე" (სს) სტრუქტურაზე დამზადებული ინტეგრალური სქემების ძირითადი უპირატესობები

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სილიციუმის ეპიტაქსიური ფენების მიღების ტექნოლოგიის განვითარებამ, რომელიც საშუალებას იძლევა მიღებულ იქნას უფრო მაღალი პარამეტრების ინტეგრალური სქემები, ვიდრე სილიციუმის მონოკრისტალურ ბლოკზე, მიგვიყვანა სტრუქტურების "სილიციუმი დიელექტრიკზე" (სდ) შექმნამდე. ამ სტრუქტურებს შორის განსაკუთრებით პერსპექტიულია ჰეტეროსტრუქტურები "სილიციუმი საფირონზე" (სს), სადაც საფირონი გამოყენებულია საფენად მასზე დაფენილ სილიციუმის ეპიტაქსიურ ფირში ინტეგრალური სქემების დასამზადებლად. ამ სქემებს გააჩნიათ შედარებით მაღალი რადიაციული მდგრადობა და სიხშირული მახასიათებლები.

სტატია ეძღვნება სს სტრუქტურებზე ინტეგრალური სქემების დამუშავებას, კერძოდ, ელექტრულად პროგრამირებად მუდმივ დამამახსოვრებელ მოწყობილობას, რომელ იც შესრულებულია ვერტიკალური დიოდური სტრუქტურების საფუძველზე.

სტატიაში აღწერილია სს სტრუქტურებზე დიოდური მატრიცის შექმნის ოპტიმალური ტექნოლოგიური მარშრუტი. დამუშავებულია საფირონზე სილიციუმის იზოლირებული პატარა "კუნძულების" მიღების ტექნოლოგია.

მოყვანილია დიოდური მატრიცის მიღების ტექნოლოგიური პარამეტრები, მოცემულია სს სტრუქტურაზე დიოდური ინტეგრალური სქემის დამზადების სრული ტექნოლოგიური ციკლი. მიღებული ელექტრულად პროგრამირებადი დიოდური მატრიცები გამოიყენებოდა კოსმოსური აპარატებისა და წყალქვეშა ნავების რადიოელექტრონულ ხელსაწყოებში, მუდმივი მახსოვრობის ბლოკში.

სტატიის ბოლოს მოყვანილია წინადადებები ნანოსილიციუმის და სს ჰეტერო-ეპიტაქსიური სტრუქტურის საფუძველზე ახალი ოპტიკურ-ელექტრონული მყარსხეულოვანი სქემების შექმნის შესახებ.

ეს წინადადებები ემყარება ბოლო წლებში ნანოზომების სილიციუმში ეფექტური გამოსხივების აღმოჩენას. საფირონზე ერთ მხარეს ნანოსილიციუმის, ხოლო მოპირდაპირე ზედაპირზე ფოტომიმღების ტექნოლოგიის დამუშავება საშუალებას იძლევა შეიქმნას სხვადასხვა სახის პერსპექტიული მყარსხეულოვანი ოპტიკურ-ელექტრონული ელემენტები და ხელსაწყოები.

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